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10EC45

Fourth Semester B.E. Degree Examination, June/July 2014

Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Mention the types of HDL descriptions. Explain how half adder can be modeled in VHDL and verilog in any one description method. **(10 Marks)**

b. Discuss the shift operators used in VHDL and verilog with example. **(04 Marks)**

c. Write switch level description of an inverter in verilog. **(03 Marks)**

d. A = 110, B = 111, C = 011000, D = 111011, evaluate A and not B or C nor 2 and D. **(03 Marks)**

2 a. Write a data flow description in VHDL for two-bit magnitude comparator. Show simulation waveforms. **(08 Marks)**

b. Write a verilog code to realize D-latch with active high enable in data flow modeling method. Show simulation waveforms. **(06 Marks)**

c. Write HDL code for 2 × 2 combinational array multiplier (VHDL or verilog). **(06 Marks)**

3 a. Write a VHDL code to realize JK flipflop with synchronous reset. **(04 Marks)**

b. Write verilog description to realize:
i) 3-bit counter using case statement
ii) 4:1 multiplexer using if statement **(06 Marks)**

c. Explain Booth algorithm with an example and write the flow chart of Booth multiplication algorithm. Write VHDL or verilog code of 4 × 4 bit Booth algorithm. **(10 Marks)**

4 a. Write the VHDL description of a 2:4 decoder using structural modeling method. **(05 Marks)**

b. Write the excitation table of an SRAM memory cell and write its structural description in VHDL or verilog. **(10 Marks)**

c. Write the structural description of a 4-bit asynchronous down counter using generate statement in verilog. **(05 Marks)**

PART – B

5 a. Write a VHDL/verilog code to convert unsigned binary to an integer using procedure/task. **(06 Marks)**

b. Write a VHDL/verilog description to find the floating sum $y = \sum_{i=0}^{3} (-1)^i (x)^i$; $0 < x < 1$ using function. **(06 Marks)**

c. Write a VHDL code to write integers to a file. **(08 Marks)**

6 a. Discuss about mixed type description and its advantages. Illustrate with an example. **(06 Marks)**

b. Write short notes on VHDL package and discuss the syntax of declaration of a package. **(07 Marks)**

c. Write the VHDL/verilog description of 16 × 8 SRAM. **(07 Marks)**

7 a. Explain how a VHDL entity can be invoked from a verilog module with full adder as an example. **(10 Marks)**

b. Write the mixed language description to invoke verilog module of JK flip-flop with clear from VHDL module. **(10 Marks)**

8 a. Discuss mapping of signal assignment statement and variable assignment statement to gate-level with suitable examples. **(05 Marks)**

b. Explain mapping of if-else statement with a suitable example. **(05 Marks)**

c. Show the synthesis information extracted from the listing shown below:

```
Package codes is
type op is (add, mul, divide, none);
end;
work codes;
entity ALUS2 is
Port (a, b: in std_logic_vector (3 downto 0);
      cin: in std_logic;
      opc: in op;
      z: out std_logic_vector (7 downto 0);
      cout: out std_logic;
      err: out Boolean);
end ALUS2;
```

(10 Marks)

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